UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/725,704	11/29/2000	Thomas J. Cloonan	4807.00017	8828

21924 7590 10/19/2005

ARRIS INTERNATIONAL, INC
3871 LAKEFIELD DRIVE
SUWANEE, GA 30024

EXAMINER	
LAMBRECHT, CHRISTOPHER M	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/725,704	CLOONAN ET AL.	
	Examiner	Art Unit	
	Christopher M. Lambrecht	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 28 July 2005 have been fully considered but they are not persuasive. In particular, Applicant submits:

a. the value "P" as discussed in Salee is not a future time value (Applicant's remarks, p. 7);

b. Salee fails to disclose copying a future timing counter value into a storage device and copying said future timing value from said storage device into said timing counter of a second circuit (Applicant's remarks, p. 7);

c. Wu does not disclose sampling and copying a first timing counter value into a storage device and adding an offset to create a future timing counter value (Applicant's remarks, p. 8);

d. the future timing counter value, as recited in the claims, is defined in the specification and includes such limitations (Applicant's remarks, p. 8);

e. because neither Salee nor Wu disclose calculating and using a future timing counter value to synchronize a plurality of CMTS circuits, or contain a suggestion to combine the references such that one skilled in the art would think of using a future timing counter value, the independent claims and their respective dependent claims are not obvious over Salee in view of Wu (Applicant's remarks, p. 8).

In response to (a), Examiner submits that the preset digital number P disclosed by Salee constitutes a future time value as claimed. In particular, master MAC chip 10 as illustrated in figure 1 comprises a system timer 24 implemented as an x-bit binary counter which increments a time value T in response to oscillations produced clock oscillator 22. Time value T represents a current time value. At some given point in time, the system determines a preset digital number P and subsequently loads P into the preset register 26 of master MAC chip 10, see ¶0013. Upon storage of preset digital number P into

preset register 26 the system monitors, by way of comparator 28, for an instant in time at which time value T, as maintained in system timer 24, is equal to preset digital number P, see ¶0014. Thus, upon storage of preset digital number P into preset register 26, the system awaits the moment in time at which time value T matches preset digital number P. There exists a non-zero interval of time (potentially as long as seven minutes, see ¶0015) that elapses between the loading of predetermined digital number P into preset register 26 and the moment at which time value T increments to a value equal to predetermined digital number P. Thus, because value T represents the current time, at the instant of the system's determination as to what value predetermined digital number P shall be (i.e., the "predetermination" of predetermined digital number P) and subsequent storage in preset register 26, predetermined digital number P represents a point in time that is later, or in the future with respect to the current time value T. Accordingly, upon its instantiation in the system and subsequent storage in preset register 26, predetermined digital number P represents "a future timing counter value."

In response to (b), Examiner submits that in light of the above remarks, Salee discloses a future timing value. Furthermore, in the context of the claims, "said future timing counter value" is a semantic identifier referencing the antecedent "a said future timing counter value," i.e., predetermined digital number P. As discussed above, P represents a future timing counter value. The language "said future timing counter value" merely references the quantity or value represented by predetermined digital number P upon its instantiation in the system of Salee, which is a future timing counter value. Therefore, Salee also discloses copying a future timing counter value (predetermined digital number P) into a storage device (preset register 26) and copying said future timing counter value (i.e., the value of predetermined digital number of P) from said storage device (26) into said timing counter (24 of MAC chip 20) of a second circuit (MAC chip 20), as set forth in the rejections of the claims in the non-final Office action.

In response to (c), Examiner submits that Applicant's arguments with respect to the alleged deficiencies of Wu appear to be predicated on the assertion that because Wu estimates time-stamp

information using a mathematical formula, Wu does not disclose calculating a future timing value based on the time it takes to process the initializing of a new circuit (Applicant's remarks, p. 8, ¶2). Initially, Examiner notes that Wu is not relied upon to teach "calculating a future timing value based on the time it takes to process the initializing of a new circuit." Even if Wu did not disclose the aforementioned limitation (which Examiner does not concede), the alleged deficiency would not prohibit Wu from disclosing copying a first timing value into a storage device and adding an offset to create a future timing counter value. Insofar as Wu is relied upon to teach creating a future timing counter value, Examiner submits that as disclosed in the cited portions of Wu, by adjusting a timing counter count value by an offset to account for delay encountered in transmitting a timestamp between to clocks, such that said clocks may be synchronized, a future timing counter value is created (i.e., one clock/counter is advanced by the offset, thus incrementing said clock/counter to a later or "future" timing value). The teachings of Wu as applied to the claimed limitations are set forth in detail in the rejection of the claims in the previous Office action. Absent a specific objection raised by Applicant as to how or why the cited portions of Wu as applied in the rejection fail to meet the claimed limitations, Examiner is unable to provide further explanation and/or clarification regarding issue (c).

In response to (d), MPEP §904.01 sets forth that for the purposes of examination, claims shall be given their broadest reasonable interpretation consistent with the specification. Examiner submits that in light of the discussion pertaining to issues (a) and (c), both Salee and Wu disclose future timing values in that these values represent future values for at least the reason that these future timing values represent values to which periodically-incrementing timing counters would or will accumulate after some non-zero time interval lapses. Furthermore, Examiner submits that the interpretation of a "future timing counter value" as any number that is greater in value than the output of a regularly-incrementing counter device is a reasonable interpretation of the claim language. As to the requirement that the interpretation of claim language maintain consistency with the specification, Examiner submits that the interpretation of the

claimed "future timing counter value" as provided in the rejections of the claims and expanded upon herein above does not depart in any way from the physical manifestation of the future timing value as described in Applicant's specification. In particular, the predetermined digital number P of Salee, the corrected timestamp of Wu, and the future timing count value of Applicant's specification all denote a predetermined number who's value is greater than that of a periodically-incrementing timing counter, at least upon said predetermined number's instantiation. Similarly, said counter thus becomes greater than or equal to the value said predetermined number at some point in the future.

As expressed in the holding of *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969), "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim,' to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." Additional limitations in association with the claimed terminology found in Applicants specification, e.g., said future timing counter value being calculating based on the measured duration of an initialization process of a new circuit, lack express basis in the claims (there is no mention in the claims of a duration of the initialization process). Thus the claimed "future timing counter value" has been given appropriate scope for examination as set forth by the MPEP and need not incorporate further limitations from Applicant's specification.

In response to (e), in light of the above remarks, Examiner submits that Salee does in fact teach calculating a future timing counter value to synchronize a plurality of CMTS and remaining claim limitations when taken in combination with the teachings of Wu as set forth in the rejections of the claims in the non-final Office action. Accordingly, Examiner submits all issues raised by Applicant regarding the rejections of the pending independent claims have been alleviated and thus these claims remain obvious over Salee in view of Wu. Additionally, absent further arguments by Applicant as to the patentability of all pending dependent claims, these claims also remain obvious as set forth in the previous Office action.

Therefore, the rejections as applied to claims 11-28 in the non-final Office action mailed 21 May 2004, and restated below, are maintained.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-15, 17, 20-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salee (of record) in view of Wu (of record).

With regard to claims 11 and 20, Salee discloses in a cable modem termination system (CMTS) (fig. 1) with a plurality of cable interface circuits (CMTS MAC chip 10, 20), each of which includes a cyclical timing counter (timer 24, ¶13, lines 13-15) that provides timing signals to cable modems coupled to each of said interface circuits (¶12, lines 6-9), a method of synchronizing the timing counter of a first cable interface circuit (20) to the timing counter of a second cable interface circuit (10) comprised of the steps of: copying a future timing counter value (preset digital number P, ¶13, lines 15-20) into a storage device (preset register 26, performed by processor, ¶14, lines 28-31); and, copying said future timing counter value from said storage device (26) into said timing counter (24, of second or "slave" circuit 20) (¶14, lines 21-25). Salee fails to explicitly disclose copying a first value of said timing counter of said first cable interface circuit into a storage device; and, adding an offset to said first value to create a future timing counter value.

In an analogous art, Wu discloses copying a first value of a timer counter (timestamp T_i) of a cable interface circuit (CMTS, col. 4, lines 55-60) into a storage device (memory, col. 6, lines 47-51); and, adding an offset (C_1) to said first value to create a future timing counter value (col. 7, lines 29-31),

for the purpose of accurately synchronizing a second local clock to a CMTS master clock (Col. 8, lines 5-11).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Salee to include copying a first value of a timer counter of a cable interface circuit into a storage device; and, adding an offset to said first value to create a future timing counter value, as taught by Wu, for the purpose of accurately synchronizing a second local clock to a CMTS master clock in a cable modem termination system.

With regard to claims 12, 13, 21, and 22, Salee and Wu together disclose the claimed subject matter. In particular, Salee discloses wherein said step of copying said future timing value (P) from said storage device (26) into said timing counter (24) includes the step of: waiting (count register is incrementing, ¶14, lines 5-10) a predetermined length of time ((preset number P) - (current timer count T)) until said timing counter is substantially equal to said future timing counter value (T=P); copying said future timing counter value (P) from said storage device (26) into said timing counter (¶14, lines 10-25).

With regard to claims 14 and 23, Salee and Wu together disclose the claimed subject matter. In particular, Salee discloses where said step of copying said future timing value (P) from said storage device (26) into said timing counter (24) includes the step of: triggering the transfer of said future timing counter value (P) from said storage device (26) into said timing counter (24) (¶14, lines 10-25) from a System Controller for said CMTS (CMTS MAC chip master 10).

With regard to claims 15 and 24, Salee discloses a cable modem termination system (CMTS) (fig. 1) with a plurality of interface circuits (CMTS MAC chips 10, 20), each of which includes a cyclical timing counter (timer 24, ¶13, lines 13-15) that provides timing signals to cable modems coupled to each

of said interface circuits (¶12, lines 6-9), said CMTS comprising: a System Controller means (master MAC chip 10) for: copying said future timing counter value (preset digital number P, ¶13, lines 15-20) from a storage device (preset register 26) into said timing counter (system timer 24) (¶14, lines 21-25). Salee fails to explicitly disclose copying a first value of said timing counter of said first cable interface circuit into a storage device; and, adding an offset to said first value to create a future timing counter value.

In an analogous art, Wu discloses copying a first value of a timer counter (timestamp T_i) of a cable interface circuit (CMTS, col. 4, lines 55-60) into a storage device (memory, col. 6, lines 47-51); and, adding an offset (C_1) to said first value to create a future timing counter value (col. 7, lines 29-31), for the purpose of accurately synchronizing a second local clock to a CMTS master clock (Col. 8, lines 5-11).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Salee to include copying a first value of a timer counter of a cable interface circuit into a storage device; and, adding an offset to said first value to create a future timing counter value, as taught by Wu, for the purpose of accurately synchronizing a second local clock to a CMTS master clock in a cable modem termination system.

With regard to claims 17 and 26, Salee and Wu together disclose the claimed subject matter. In particular, Salee discloses said system controller is an application specific integrated circuit (MAC chip master 10, where a chip is an integrated circuit).

4. Claims 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salee and Wu as applied to claims 15 and 24 above, and further in view of Quigley (of record).

With regard to claims 16 and 25, Salee and Wu fail to disclose said system controller is a microprocessor.

Quigley discloses a system controller (TDMA controller 3004, fig. 80) is a microprocessor (¶550, lines 10-15), for the purpose of enabling programming of the system controller (¶550, lines 10-15).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Salee and Wu to include said system controller is a microprocessor, as taught by Quigley, for the purpose of enabling programming of the system controller in a cable modem termination system.

5. Claims 18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salee and Wu as applied to claim 15 and 24 above, and further in view of Wang (of record).

With regard to claims 18 and 27, Salee and Wu fail to explicitly disclose said System Controller is a field programmable gate array (FPGA).

In an analogous art, Wang discloses a system controller (processing unit) is a FPGA (programmable logic device 121, fig. 1), for the purpose of providing the advantages of fixed integrated circuits with the flexibility of custom integrated circuits (¶28, lines 6-13).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Salee and Wu to include said system controller is a FPGA, as taught by Wang, for the purpose of providing the advantages of fixed integrated circuits with the flexibility of custom integrated circuits in a cable modem termination system.

6. Claims 19 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salee and Wu as applied to claim 15 and 24 above, and further in view of Florine (of record).

With regard to claims 19 and 28, Salee and Wu fail to disclose said System Controller is sequential logic.

In an analogous art, Florine discloses a system controller is sequential logic (col. 9, lines 32-36) for the purpose of providing flexibility and predictability (col. 9, lines 32-36).

Consequently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Salee and Wu to include said system controller is sequential logic, as taught by Florine, for the purpose of providing flexibility and predictability in a cable modem termination system.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually depositing or transmitting the correspondence or by an individual who, upon information and belief, expects the correspondence to be mailed or transmitted in the normal course of business by another no later than the date indicated.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on _____.
(Date)

Typed or printed name of person signing this certificate:

_____

Signature: _____

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (703)_____ - _____ on _____.
(Date)

Typed or printed name of person signing this certificate:

_____

Signature: _____

Please refer to 37 CFR 1.6(d) and 1.8(a)(2) for filing limitations concerning facsimile transmissions and mailing, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Lambrecht whose telephone number is (571) 272-7297. The examiner can normally be reached on 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the primary examiner, Christopher Grant can be reached on (571) 272-7294. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher M Lambrecht
Examiner
Art Unit 2611

CML

HAI TRAN
PRIMARY EXAMINER